
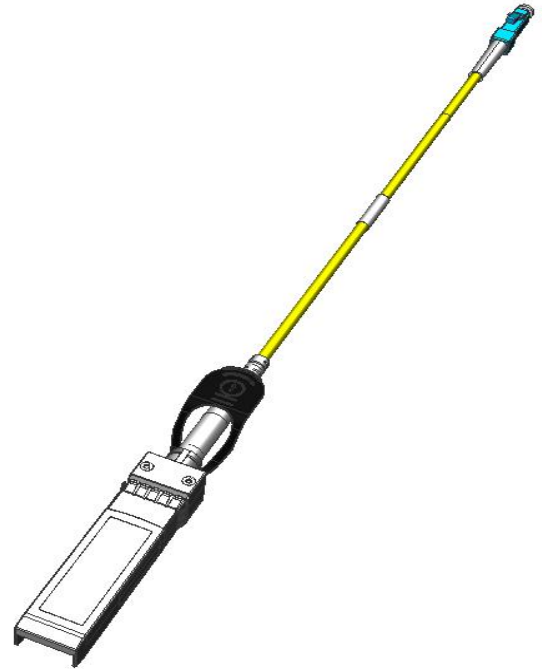


## 25Gbps SFP28 Bi-Directional Transceiver for liquid immersion **GL-S1250LR-XXX**

### Features

- ✓ Hot-pluggable SFP28 form factor
- ✓ Up to 25Gbps data rate and maximum link length of Bi-directional 10km
- ✓ Customized length pigtail and single receptacle
- ✓ CWDM DFB laser and PIN photo-detector  
1270nm Tx/1330nm Rx
- ✓ Internal CDR on both Transmitter and Receiver channel
- ✓ Single 3.3V power supply
- ✓ Power dissipation < 1.6W
- ✓ RoHS compliant and lead free 
- ✓ Operating case temperature: 0°C to 60°C or more



### Applications

- ✓ 25GBASE-LR Ethernet
- ✓ CPRI Option 10
- ✓ Support 10G CPRI option 8 by CDR bypass
- ✓ Liquid immersion environment

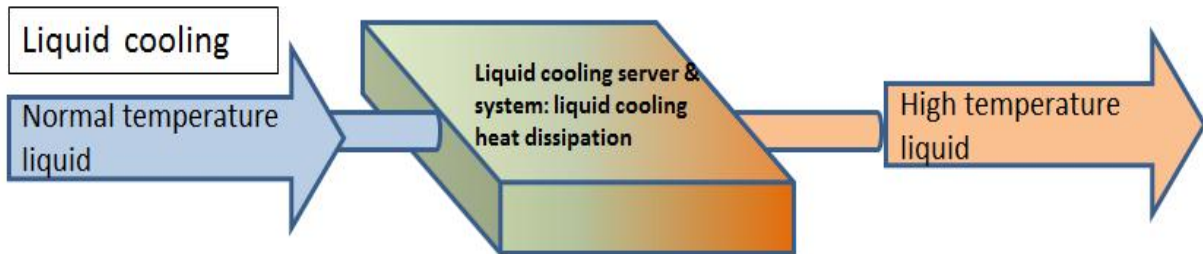
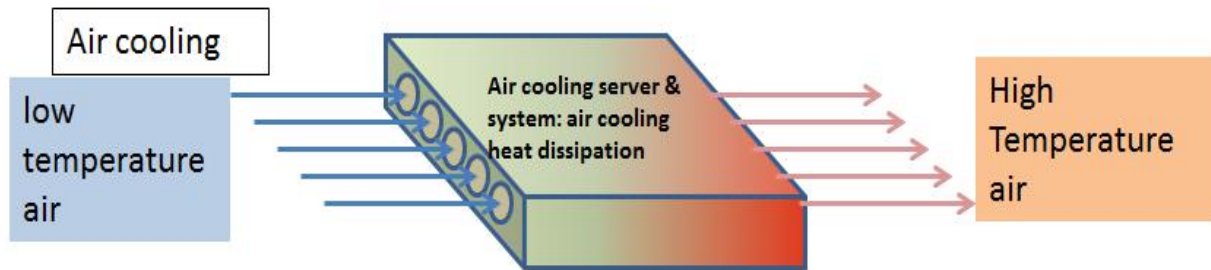
### Description

The Gigalight Technologies GL-S1250LR-XXX is designed for Bi-directional 25G serial optical data communications by using 1270nm transmitter and 1330nm receiver, it is a high performance module for 25G Ethernet and Option 10 CPRI applications which operate up to 10km. This module incorporates Gigalight Technologies proven circuit and technology to provide reliable long life, high performance, and consistent service.

GL-S1250LR-XXX depends on reliable sealed design to enable the module for liquid immersion environment, this product can be customized the length of pigtail and receptacle to adapt the variety of requirement.

## Liquid immersion Advantage

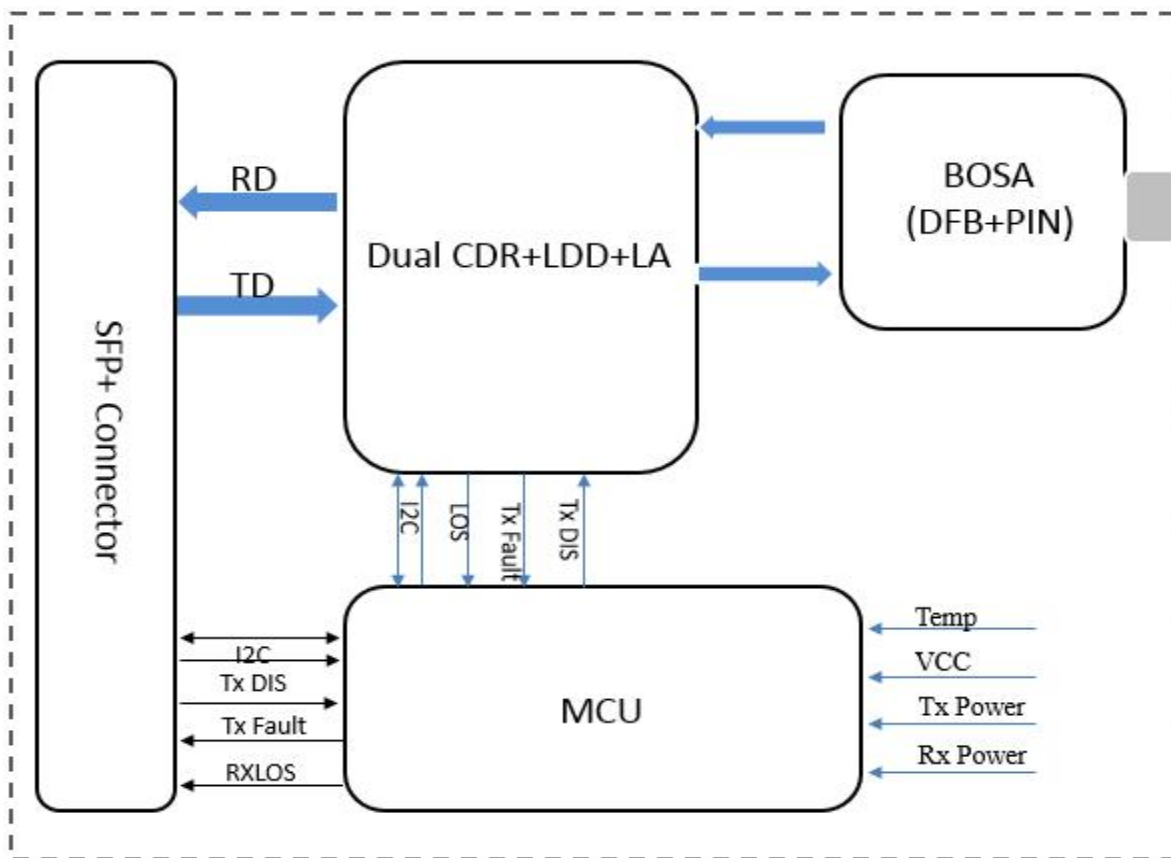
### Air cooling compare liquid cooling



As the requirement of data traffic keeping growth and the heat flux emitted by datacenter internal chips increases constantly, traditional air cooling methods are under pressure. Liquid cooling technologies removes the heat more efficiently with dielectric fluids that have high heat capacity to improve the efficiency of energy in datacenter.

Gigalight solved the lack of optical transceivers which perform reliability in immersion even liquid immersion depth up to 10m, the Liquid cooling optical series transceiver is suitable for liquid cooling server & system, this series product are compatible with fluorinated liquid and mineral oils well.

## Block Diagram



## Absolute Maximum Ratings

| Parameter           | Symbol | Min | Max | Unit |
|---------------------|--------|-----|-----|------|
| Supply Voltage      | Vcc    | 0   | 3.6 | V    |
| Storage Temperature | Ts     | -40 | +85 | °C   |
| Operating Humidity  | -      | 5   | 85  | %    |

## Recommended Operating Conditions

| Parameter                  | Symbol | Min  | Typical | Max  | Unit |
|----------------------------|--------|------|---------|------|------|
| Operating Case Temperature | Tc     | 0    |         | 60   | °C   |
| Power Supply Voltage       | Vcc    | 3.13 | 3.3     | 3.47 | V    |
| Power Supply Current       | Icc    |      |         | 485  | mA   |
| Liquid immersion depth     |        |      |         | 10   | m    |

## Electrical Specifications

| Parameter                              | Symbol           | Min                  | Typical | Max             | Unit  |
|--|------------------|----------------------|---------|-----------------|-------|
| Differential Input Impedance           | Zin              | 90                   | 100     | 110             | ohm   |
| Differential Output Impedance          | Zout             | 90                   | 100     | 110             | ohm   |
| Differential Input Voltage Amplitude1  | $\Delta V_{in}$  | 300                  |         | 1100            | mVp-p |
| Differential Output Voltage Amplitude2 | $\Delta V_{out}$ | 500                  |         | 800             | mVp-p |
| Input Logic Level High                 | V <sub>IH</sub>  | 2.0                  |         | V <sub>cc</sub> | V     |
| Input Logic Level Low                  | V <sub>IL</sub>  | 0                    |         | 0.8             | V     |
| Output Logic Level High                | V <sub>OH</sub>  | V <sub>cc</sub> -0.5 |         | V <sub>cc</sub> | V     |
| Output Logic Level Low                 | V <sub>OL</sub>  | 0                    |         | 0.4             | V     |

### Note:

- 1、Differential input voltage amplitude is measured between TxnP and TxnN.
- 2、Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

| Parameter                    | Symbol                             | Min | Typical | Max | Unit | Notes |
|------------------------------|------------------------------------|-----|---------|-----|------|-------|
| <b>Transmitter</b>           |                                    |     |         |     |      |       |
| Data rate                    | BR                                 |     | 25.78   |     | Gbps |       |
| Centre Wavelength            | $\lambda_c$                        |     | 1270    |     | nm   |       |
| Spectral Width (-20dB)       | $\sigma$                           |     |         | 1   | nm   |       |
| Side Mode Suppression Ratio  | SMSR                               | 30  |         |     | dB   |       |
| Average Output Power         | P <sub>avg</sub>                   | -2  |         | 6   | dBm  |       |
| Optical Modulation Amplitude | OMA                                | -4  |         | 6   | dBm  |       |
| Extinction Ratio             | ER                                 | 3   |         |     | dB   |       |
| Eye Mask Coordinates         | {0.31, 0.4, 0.45, 0.34, 0.38, 0.4} |     |         |     |      |       |
| <b>Receiver</b>              |                                    |     |         |     |      |       |
| Data rate                    | BR                                 |     | 25.78   |     | Gbps |       |
| Centre Wavelength            | $\lambda_c$                        |     | 1330    |     | nm   |       |
| Average Power at Receiver    |                                    |     |         | 3   | dBm  |       |
| Receive reflectance(max)     |                                    |     |         | -26 | dB   |       |

|                                    |                  |     |   |       |     |   |
|------------------------------------|------------------|-----|---|-------|-----|---|
| Receiver Sensitivity (OMA)         | Psens            | -   | - | -12.0 | dBm | 1 |
| Stressed receiver sensitivity(OMA) |                  |     |   | -9.5  | dBm | 2 |
| LOS De-Assert                      | LOS <sub>D</sub> |     |   | -12   | dBm |   |
| LOS Assert                         | LOS <sub>A</sub> | -30 |   |       | dBm |   |
| LOS Hysteresis                     |                  | 0.5 |   |       | dB  |   |

**Note:**

- 1、 For 25G-LR with FEC, receiver sensitivity is defined at 5E-5 BER level, not 10-12 BER level.
- 2、 Measured with conformance test signal at TP3 for BER=5E-5.

**Timing and Electrical**

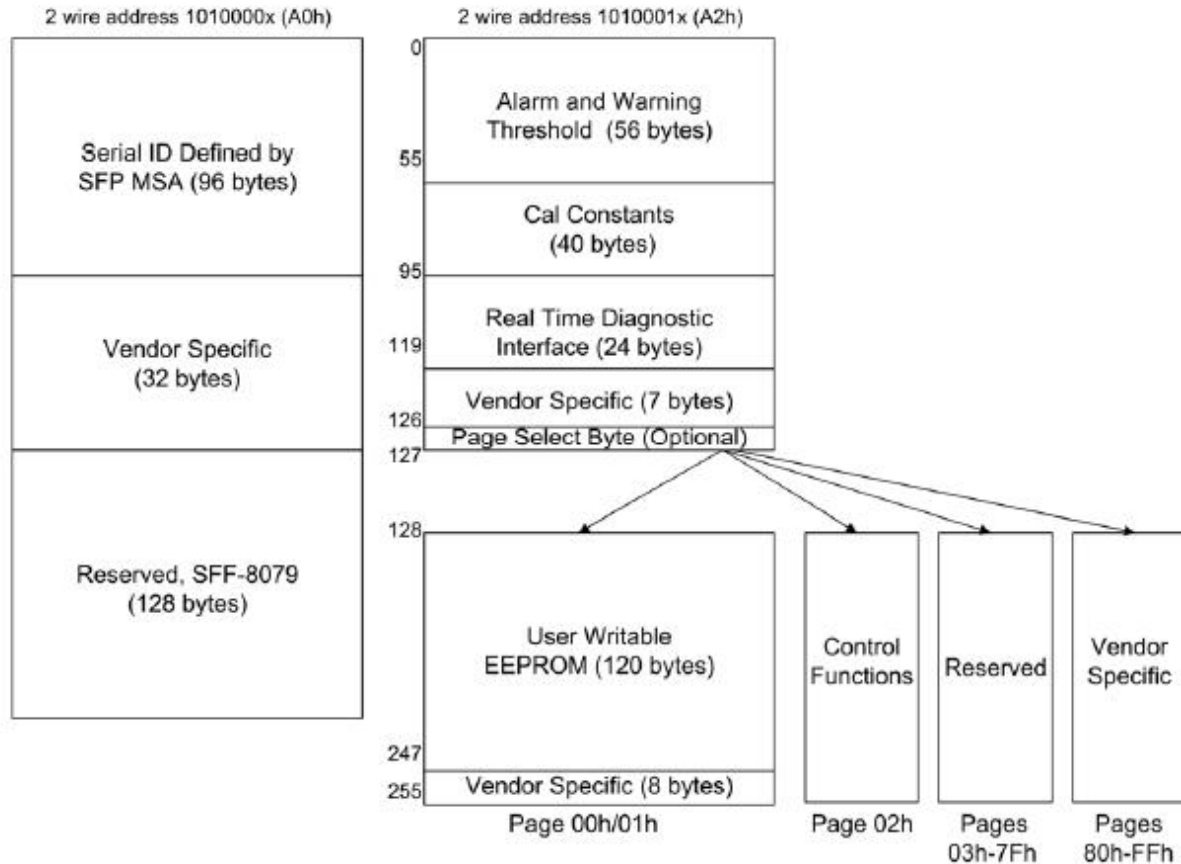
| Parameter   | Symbol             | Min. | Max. | Unit | Conditions   |
|---|--------------------|------|------|------|--|
| Tx_Disable assert time  | t_off              |      | 100  | μs   | Rising edge of Tx_Disable to fall of output signal below 10% of nominal  |
| Tx_Disable negate time  | t_on               |      | 2    | ms   | Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.  |
| Time to initialize 2-wire interface   | t_2w_start_up      |      | 300  | ms   | From power on or hot plug after the supply meeting Table 8.  |
| Time to initialize  | t_start_up         |      | 300  | ms   | From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.   |
| Time to initialize cooled module and time to power up a cooled module to Power Level II | t_start_up_cooled  |      | 90   | s    | From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational |
| Time to Power Up to Level II  | t_power_level2     |      | 300  | ms   | From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational  |
| Time to Power Down from Level II  | t_power_down       |      | 300  | ms   | From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements  |
| Tx_Fault assert   | Tx_Fault_on        |      | 1    | ms   | From occurrence of fault to assertion of Tx_Fault  |
| Tx_Fault assert for cooled module   | Tx_Fault_on_cooled |      | 50   | ms   | From occurrence of fault to assertion of Tx_Fault  |
| Tx_Fault Reset  | t_reset            | 10   |      | μs   | Time Tx_Disable must be held high to reset Tx_Fault  |
| RS0, RS1 rate select timing for FC  | t_RS0_FC, t_RS1_FC |      | 500  | μs   | From assertion till stable output  |
| RS0, RS1 rate select timing non FC  | t_RS0, t_RS1       |      | 24   | ms   | From assertion till stable output  |
| Rx_LOS assert delay   | t_los_on           |      | 100  | μs   | From occurrence of loss of signal to assertion of Rx_LOS   |
| Rx_LOS negate delay   | t_los_off          |      | 100  | μs   | From occurrence of presence of signal to negation of Rx_LOS  |

## Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

The memory map specific data field defines as following.

### Two-wire Interface Fields



### TWO-WIRE INTERFACE FIELDS

## CDR Rate Select control

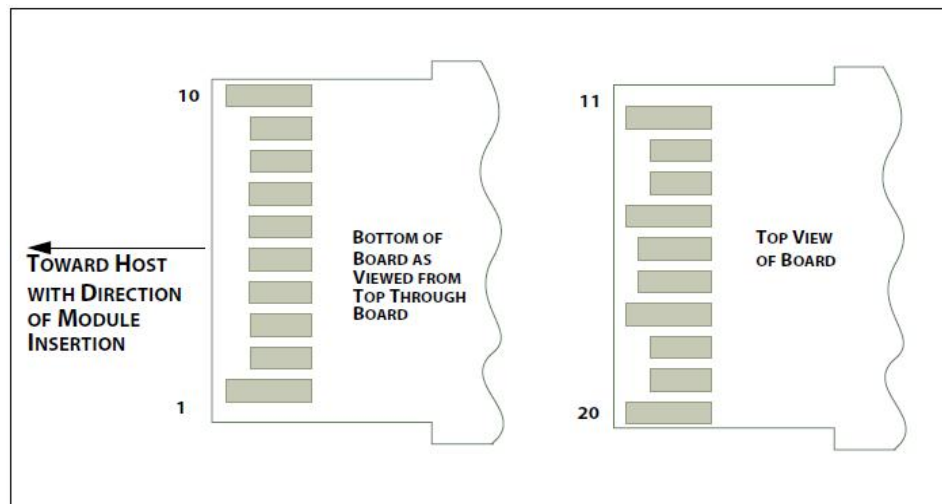
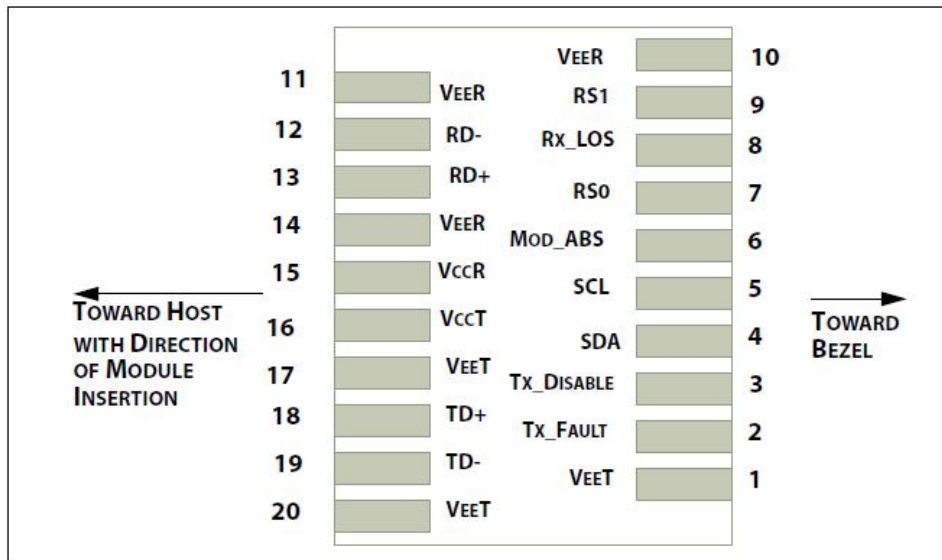
The soft RS(0) select bit(A2h byte 110 bit3) and soft RS(1) select bit(A2h byte118 bit3) are CDR control bits that allow for the CDR Rate Select using the 2-wire interface. These bits and the corresponding rate select pins RS0 and RS1 are connected through a logical OR function so that the CDR is controled when either the bit is “1” or the pin is “high”.

**TABLE 10-2 RETIMER/CDR RATE SELECT LOGIC TABLE**

| When byte 13d of A0h is set to 0Eh and bit 64.3 of A0h is set to 1 |                                 |                       |                         |
|--|---------------------------------|-----------------------|-------------------------|
| Logic OR of RS0 pin and RS0 bit                                    | Logic OR of RS1 pin and RS1 bit | Receiver retimer/CDR  | Transmitter retimer/CDR |
| Low/0  | Low/0                           | Lock at low bit rate  | Lock at low bit rate    |
| Low/0  | High/1                          | Lock at high bit rate | Bypass                  |
| High/1   | Low/0                           | Bypass                | Bypass                  |
| High/1   | High/1                          | Lock at high bit rate | Lock at high bit rate   |

Note: Low and high bit rates are defined in byte 13d of A0h.

### Pin Definitions



## Pin Descriptions

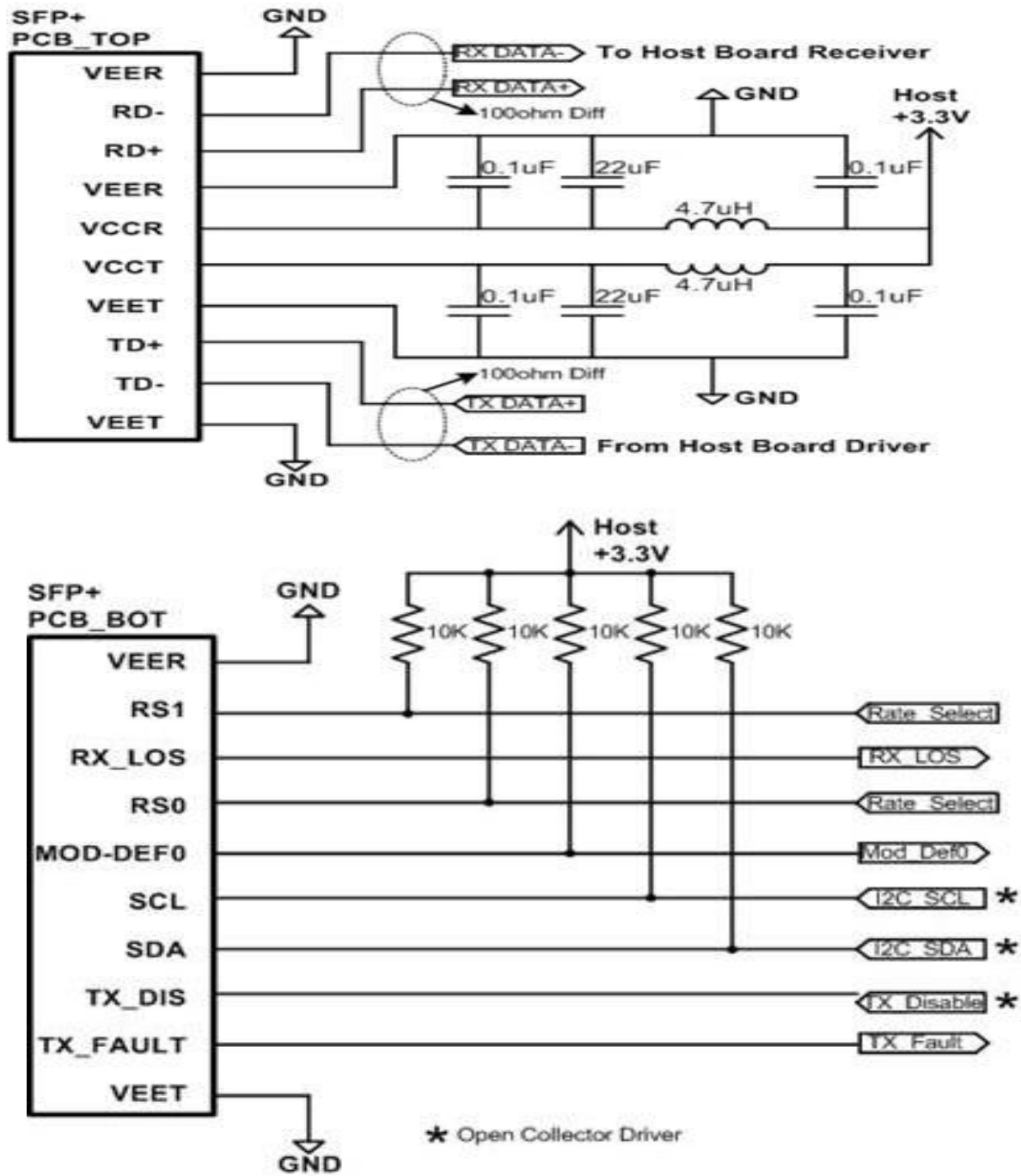
| PIN | Logic     | Symbol   | Name / Description                                      | Note |
|-----|-----------|----------|---|------|
| 1   |           | VeeT     | Module Transmitter Ground                               | 1    |
| 2   | LVTTL-O   | TX_Fault | Module Transmitter Fault                                | 2    |
| 3   | LVTTL-I   | TX_Dis   | Transmitter Disable; Turns off transmitter laser output |      |
| 4   | LVTTL-I/O | SDA      | 2-Wire Serial Interface Data Line                       | 2    |
| 5   | LVTTL-I   | SCL      | 2-Wire Serial Interface Clock                           | 2    |
| 6   |           | MOD_ABS  | Module Definition, Grounded in the module               |      |
| 7   | LVTTL-I   | RS0      | Receiver Rate Select                                    |      |
| 8   | LVTTL-O   | RX_LOS   | Receiver Loss of Signal Indication Active LOW           |      |
| 9   | LVTTL-I   | RS1      | Transmitter Rate Select (not used)                      |      |
| 10  |           | VeeR     | Module Receiver Ground                                  | 1    |
| 11  |           | VeeR     | Module Receiver Ground                                  | 1    |
| 12  | CML-O     | RD-      | Receiver Inverted Data Output                           |      |
| 13  | CML-O     | RD+      | Receiver Data Output                                    |      |
| 14  |           | VeeR     | Module Receiver Ground                                  | 1    |
| 15  |           | VccR     | Module Receiver 3.3 V Supply                            |      |
| 16  |           | VccT     | Module Receiver 3.3 V Supply                            |      |
| 17  |           | VeeT     | Module Transmitter Ground                               | 1    |
| 18  | CML-I     | TD+      | Transmitter Non-Inverted Data Input                     |      |
| 19  | CML-I     | TD-      | Transmitter Inverted Data Input                         |      |
| 20  |           | VeeT     | Module Transmitter Ground                               | 1    |

### Notes:

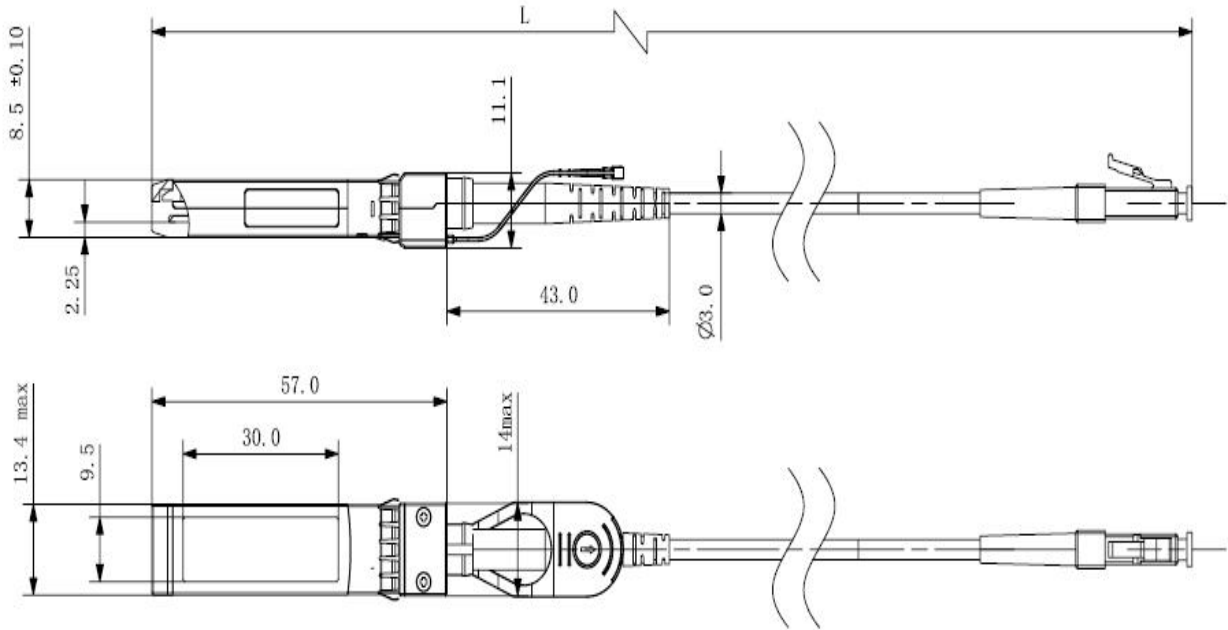
- 1.Module ground pins GND are isolated from the module case.
- 2.Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.



### Recommended Interface Circuit



## Mechanical Dimensions



## Regulatory Compliance

Gigalight GBP-2733250-LRT transceivers are Class 1 Laser Products. They meet the requirements of the following standards:

| Feature                  | Standard   |
|--------------------------|--|
| Laser Safety             | IEC 60825-1:2014 (3 <sup>rd</sup> Edition)<br>IEC 60825-2:2004/AMD2:2010<br>EN 60825-1:2014<br>EN 60825-2:2004+A1+A2 |
| Electrical Safety        | EN 62368-1: 2014<br>IEC 62368-1:2014<br>UL 62368-1:2014  |
| Environmental protection | Directive 2011/65/EU with amendment(EU)2015/863  |
| CE EMC                   | EN55032: 2015<br>EN55035: 2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013   |
| FCC                      | FCC Part 15, Subpart B; ANSI C63.4-2014  |

## References

1. SFP28 MSA
2. Ethernet IEEE802.3cc
3. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.

### CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Ordering information

| Part Number   | Product Description  |
|---|--|
| GL-S1250LR- <del>XXX</del><br>X:receptacle type,F=FC;S=SC;L=LC<br>XX: pigtail length in meters, 01/02/... | 25Gbps, 1270nm Tx/1330nm Rx; SFP28, 10km<br>Bi-direction, liquid immersion |

For example: GL-S1250LR-L03 is 25G Bi-direction liquid immersion transceiver with LC receptacle pigtail and the length is 3 meters.

## Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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## Revision History

| Revision | Date        | Description      |
|----------|-------------|------------------|
| V0       | Jul-31-2023 | Advance Release. |